Amendments to the Specification:

Please replace the paragraph that starts on page 15, line 5, with the following amended paragraph:

The instruction decoder and execution unit 210 receives an instruction stream 215 from an instruction fetch unit. The instruction stream 215 includes a number of instructions. The instruction decoder and execution unit 210 decodes the instructions and executes the decoded instructions. These instructions may be at the micro- or macro- level. The instruction decoder and execution unit 210 may be a physical circuit or an abstraction of a process of decoding and execution of instructions. In addition, the instructions may include isolated instructions and non-isolated instructions. The instruction decoder and execution unit 210 generates a virtual address 212 when there is an access transaction. The TLB 218 translates the virtual address 212 into a physical address which is part of access information 226. The instruction ~~decoeder~~ decoder and execution unit 210 interfaces with the isolated bus cycle generator 220 via control/status information 222 and operand 224. The control/status information 222 includes control bits to manipulate various elements in the isolated bus cycle generator 220 and status data from the isolated bus cycle generator 220. The operand 224 includes data to be written to and read from the isolated bus cycle generator 220. The access information 226 includes address, read/write, and access type information.

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Please replace the paragraph that starts on page 16, line 3, with the following amended paragraph:

Figure 2B is a diagram illustrating the isolated bus cycle generator 220 shown in Figure 2A according to one embodiment of the invention. The isolated bus cycle generator 220 includes a configuration storage 250, an access generator circuit 270, and a bus cycle decoder 280. The isolated bus cycle generator 220 exchanges operand 224 with, and receives the access information 226 from, the instruction decoder and execution unit 210 shown in Figure 2A. The access information 226 includes a physical address 282, a read/write (RD/WR#) signal 284 and an access type 286. The access information 226 is generated during an access transaction by the processor 110.

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